2025 International Conference on Analog VLSI Circuits (AVIC 2025)

Matsue, Japan, Oct. 20–22, 2025

Tentative Program

Organised & Sponsored by

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Conference Time Table

October 20, 2025 (Monday) — Japan Standard Time (UTC+9)

Start	End	
12:00	17:00	Registration
13:00	13:10	Opening Ceremony
13:10	14:10	Keynote 1: Prof. Nazrul Anuar bin Nayan Chair: Assoc. Prof. Yasuhiro Takahashi
14:10	14:20	Coffee break
14:20	16:20	Regular Session 1: Energy Harvesting and Analog Circuit Applications Chair: TBD
16:20	16:30	Coffee break
16:30	18:10	Regular Session 2: Application Circuits for RF & Optical Communications Chair: TBD

October 21, 2025 (Tuesday)

Start	End	
9:00	10:00	Keynote 2: Prof. François Rivet Chair: Prof. Kawori Sekine
10:00	10:10	Coffee break
10:10	12:10	Regular Session 3: Power Circuits Chair: TBD
12:10	13:30	Lunch Time
13:30	17:30	Excursion: Adachi Museum (After the excursion, we will go directly to the banquet venue by bus.)
18:00	20:00	Banquet (Venue: 日本庭園由志園, Japanese Garden Yushi-en)

October 22, 2025 (Wednesday)

Start	End	
9:00	10:00	Keynote 3: Prof. Toshihiko Hamasaki Chair: Prof. Fujihiko Matsumoto
10:00	10:10	Coffee Break
10:10	12:10	Regular Session 4: Nonlinear Analog Circuits & Signal Processing Chair: TBD
12:10	12:20	Closing Ceremony

Keynote

Monday October 20 13:10—14:10

Chairman: Yasuhiro Takahashi (Gifu University)

Speaker **Prof. Nazrul Anur bin Nayan, Universiti Kebangsaan Malaysia (UKM), Malaysia**

Title **Smarter signals for healthier lives**

Abstract Signals from the body such as electrocardiogram (ECG), photoplethysmogram (PPG), and glucose levels carry important information about health. These signals are often small and affected by noise. With the use of advanced analog front-end circuits, ECG and PPG signals can be cleaned and shaped before reaching digital processing. This allows artificial intelligence to work more accurately and with much lower power. When applied to wearable monitors and glucose sensors, these techniques support continuous and real-time health tracking. In this talk, the combination of circuit design and intelligent signal processing will be introduced as a way to create simpler and more effective diagnostic systems for everyday use.

Biography Dr. Nazrul Anuar Nayan is a Researcher at the Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia (UKM), where he has served since 2008. His research focuses on biomedical signal processing and microelectronics. He is also the CEO of IDNA Ideas, a UKM start-up company dedicated to technology training and engineering education. Dr. Nazrul is a registered Professional Engineer with the Board of Engineers Malaysia since 2013. Prior to his academic career, he gained industry experience in engineering design and semiconductor manufacturing at Hitachi Ltd. Japan, Unisem, and Stats ChipPAC. From 2014 to 2016, he conducted postdoctoral research at the Institute of Biomedical Engineering, University of Oxford, where he was also a Research Member of Common Room at Kellogg College. He holds a B.Eng. from The University of Tokyo (1998), and an M.Eng. (2008) and D.Eng. (2011) in Electronics and Information Systems from Gifu University, Japan.

Keynote

Tuesday October 21 9:00–10:00

Chairman: Kawori Sekine (Meiji University)

Speaker Prof. François Rivet, Université de Bordeaux, France

Title Let's connect intelligences

Abstract Who remembers a world without cell phones and the Internet? Radio Frequency Integrated Circuits (RFIC) have enabled democratizing communications with ever-greater data exchanges. We invent the technology and systems that allow us to increase the communication potential from one generation to the next tenfold: goodbye 4G, we are making 5G with 6G in our sights and even beyond. What more can we connect and how? Human and artificial intelligences will communicate in tomorrow's networks with integrated circuits we will invent now.

Biography Dr. François Rivet received his Master's and Ph.D. degrees in 2005 and 2009 from the University of Bordeaux. Since June 2010, he has been tenured as an Associate Professor at the Bordeaux Institute of Technology (Bordeaux INP). His research is focused on the design of RFICs in the IMS Laboratory, the University of Bordeaux microelectronics laboratory. In 2014, he founded the "Circuits and Systems" research team. Dr. Rivet has publications in top-ranked journals, international, and national conferences and holds 20 patents. He is involved in several Technical Program Committees (RFIC, ESSCIRC, ...) and in steering committees (RFIC, ICECS, LASCAS). He is a member of the Board of Governors of the IEEE Circuits and Systems Society since 2024.

Keynote

Wednesday October 22 9:00–10:00

Chairman: Fujihiko Matsumoto (National Defense Academy)

Speaker **Prof. Toshihiko Hamasaki, Hiroshima Institute of Technology, Japan**

Title **Power, precision, and intelligence: The future of audio in the age of generative AI**

Abstract This presentation explores the evolving landscape of professional and high-end consumer audio equipment, focusing on the interplay between analog fidelity, digital innovation, and emerging AI technologies. Drawing from decades of experience in designing world-class DAC/ADC chips, the talk highlights how boundary devices—those bridging analog and digital realms—remain critical to audio quality and inherently power-intensive. As generative AI enters the audio domain, from mixing consoles to guitar emulators, we examine how its computational demands influence design choices, power budgets, and creative possibilities. The session will also address sustainability, user experience, and the future of audio craftsmanship in an increasingly intelligent ecosystem.

Biography Dr. Hamasaki received his Doctor of Engineering degree in 1984 from Hiroshima University, where he conducted advanced research on hydrogenated amorphous silicon using plasma CVD technology. His work was part of Japan's national "Sunshine Project," a major initiative led by the Ministry of International Trade and Industry. From 1984 to 1991, he worked at Toshiba's ULSI Research Center, participating in the government-sponsored "Three-Dimensional IC" project. He later focused on high-precision SPICE modeling of high-speed bipolar transistors, contributing to the advancement of semiconductor simulation technologies. In 1991, Dr. Hamasaki joined Burr-Brown Corporation as Development Director for the Consumer Product Line. He led the design of mixed-signal semiconductor systems for audio and imaging applications, managing a cross-functional development team. Following Burr-Brown's acquisition, he became Head of the Analog Technology Center at DCES Company of Texas Instruments Ltd. from 2001 to 2010. In recognition of his technical excellence and leadership, he was honored with the TI Fellow Award in 2004. From 2010 to 2024, Dr. Hamasaki served as Professor at Hiroshima Institute of Technology, where he held key leadership roles including Dean of the Faculty of Applied Information Sciences and Director of the IoT Technology Research Center. His research continued to explore the frontier between analog and digital signal processing, while

also promoting the development of talent for industrial digital transformation and advancing IoT technologies in regional industries. Dr. Hamasaki is a Senior Member of both the IEEE and the Institute of Electronics, Information and Communication Engineers (IEICE). He has actively contributed to academic communities, serving as Vice Chair of the IEICE Technical Committee on Integrated Circuits and Devices and Chair of the IEEJ Technical Meeting on Electronic Circuits.

Regular Session

Monday October 20 14:20–16:20

Session 1: Energy Harvesting and Analog Circuit Applications

Chairman: TBD

A1 Low-power SEAL-RF adiabatic logic circuit with DC bias power supply
Marina Shibata, Yasuhiro Takahashi (Gifu University, Japan)*

A2 The SSHC compaction method using capacitor reusing technique
Yusuke Kakinuma, Ryoichi Miyauchi, Akira Hyogo (Tokyo University of Science, Japan)*

A3 A design of a new lossy FDNR employing VCII
Daichi Shigihara, Fujihiko Matsumoto, Kazuki Hatai (National Defence Academy, Japan)*

A4 A method to construct FDNR without requiring capacitance matching and its application to low-frequency LPF
Tsuyoshi Ito, Takashi Nishi, Fujihiko Matsumoto (National Defence Academy, Japan)*

A5 Analog LSI design platform for open source silicon development and porting
Seijiro Moriyama (Anagix Corporation, Japan); Chikau Takahashi (Takamori Co., Ltd., Japan); Kazuhiro Shouno (University of Tsukuba, Japan); Hiroshi Tanimoto (Kitami Institute of Technology, Japan); Shingo Ura, Tadaaki Tsuchiya (Logic Research Co., Ltd., Japan)*

A6 High-speed a four-armed bandit problem solving IC in CMOS 180 nm technology
Tomoki Furuta, Rin Tsuboi, Kawori Sekine, Kazuyuki Wada (Meiji University, Japan); Shinsuke Hara, Satoru Tanoi, Akifumi Kasamastu (National Institute of Information and Communications Technology, Japan)*

Monday October 20 16:30–18:10

Session 2: Application Circuits for RF & Optical Communications

Chairman: TBD

B1 High-efficiency walsh LMS-based digital predistortion RF power amplifiers
Maxandre Fellmann, François Rivet, Nathalie Deltimple, Pierre Ferrer, Rémi Quéheille, Hervé Lapuyade, Yann Deval, Eric Kerhervé (Université de Bordeaux, France)*

B2 25-28 GHz push-push VCO with flicker noise suppression circuits
Hiyori Kishimoto, Kiyotaka Komoku, Jun Furuta, Yasunori Suzuki, Nobuyuki Itoh (Okayama Prefectural University, Japan)*

B3 A proposed TIA circuit based on INV-TIA and RGC-TIA
Kento Samura, Yasuhuiro Takahashi (Gifu University, Japan)*

B4 A high-gain 25-Gb/s active voltage current feedback transimpedance amplifier in 65-nm CMOS
Yudai Taki, Yasuhuiro Takahashi (Gifu University, Japan)*

B5 An energy-efficient 25-Gb/s common gate feedforward transimpedance amplifier
Hikaru Matsunami, Yasuhuiro Takahashi (Gifu University, Japan)*

Tuesday October 21 10:10–12:10

Session 3: Power Circuits

Chairman: TBD

C1 A 728 mV and 23.4 ppm/°C voltage reference using parasitic diode biasing for temperature compensation in 28 nm FD-SOI technology
Maxime Guillot, Yann Deval, Hervé Lapuyade, François Rivet (Université de Bordeaux, France)*

C2 PTAT voltage generater-based voltage reference circuit without external bias voltage
Emu Murata, Kawori Sekine, Shuya Isawa, Michitaka Yoshino, Kazuyuki Wada (Meiji University, Japan); Hervé Lapuyade, François Rivet, Yann Deval (Université de Bordeaux, France)*

C3 Thermal profile on IC employing PTAT voltage generator consisting of two MOSFETs
Keita Hasegawa, Michitaka Yoshino, Kawori Sekine, Kazuyuki Wada (Meiji University, Japan)*

C4 Design and measurement of voltage reference circuit by an equivalent MOSFET having different temperature coefficient of threshold voltage
Shuya Isawa, Michitaka Yoshino, Kawori Sekine, Kazuyuki Wada (Meiji University, Japan); François Rivet, Hervé Lapuyade, Yann Deval (Université de Bordeaux, France)*

C5 Applying gate–source voltage enhancement and threshold voltage reduction techniques to ultra-low voltage charge-pump circuit
Arisa Shimizu, Ryoichi Miyauchi, Akira Hyogo (Tokyo University of Science, Japan)*

C6 Active CMOS rectifier circuits with wide input voltage range
Nicodimus Retdian (Shibaura Institute of Technology, Japan)*

Wednesday October 22 10:10–12:10

Session 4: Nonlinear Analog Circuits & Signal Processing

Chairman: TBD

D1 A symmetrical STDP circuit suitable for low-power P-HCNM and time-series pattern recall in a fully connected hopfield network
Ryosuke Ohnuma, Yoshiki Sasaki (Nihon University, Japan)*

D2 A study on feedback architecture for STDP learning in hierarchical neural networks using P-HCNM
Fuya Imamura, Yoshiki Sasaki (Nihon University, Japan)*

D3 A study on reducing processing time by narrowing down target vehicles in a BLE-based intersection collision prevention system
Hinata Murakoshi, Yoshiki Sasaki (Nihon University, Japan)*

D4 A spike timing dependent plasticity learned feedback network in reservoir computing for time-series pattern recognition
Akinobu Yamaguchi, Yoshiki Sasaki (Nihon University, Japan)*

D5 A study on yield improvement of low-voltage P-HCNM as spiking neuron circuit with latch-up countermeasures
Yoshiki Sasaki (Nihon University, Japan)

D6 A study on reservoir computing using a single P-HCNM with self-feedback
Ryo Ono, Takeru Yonekawa, Takuto Yamaguchi, Katsutoshi Saeki (Nihon University, Japan)*

Note: * is a presenter.