2025 International Conference on Analog VLSI Circuits

October 20 (Mon) - October 22 (Wed) 2025, Matsue, Japan

Tentative Timetable Japan Standard Time (UTC+9)

October 20, 2025 (Monday)

Start	End	
12:00	17:00	Registration
13:00	13:10	Opening Ceremony
13:10	14:10	Keynote 1 Chair: TBD
14:10	14:20	Coffee break
14:20	16:20	Regular Session 1 Chair: TBD
16:20	16:30	Coffee break
16:30	17:50	Regular Session 2 Chair: TBD

October 21, 2025 (Tuesday)

Start	End	
9:00	10:00	Keynote 2 Chair: TBD
10:00	10:10	Coffee break
10:10	12:10	Regular Session 3 Chair: TBD
12:10	13:30	Lunch Time
13:30	17:30	Excursion: Adachi Museum (After the excursion, we will go directly to the banquet venue by bus.)
18:00	20:00	Banquet (日本庭園由志園, Japanese Garden Yushi-en)

October 22, 2025 (Wednesday)

Start	End	
9:00	10:00	Keynote 3 Chair: TBD
10:00	10:10	Coffee Break
10:10	12:10	Regular Session 4 Chair: TBD
12:10	12:20	Closing Ceremony